CLAIMS

1. A clock recovery circuit for recovering a symbol clock from an input signal, comprising:

an N-interval detection unit operable to detect an N zero-crossing interval with reference to N+1 zero-crossing signals obtained from the input signal, where N is an integer greater than or equal to 2;

a judgment unit operable to judge whether the N zero-crossing interval is within a predetermined interval range; and

a clock generation unit operable to generate a symbol clock based on a result of the judgment.

2. The clock recovery circuit of claim 1, wherein the clock generation unit uses the N+1 zero-crossing signals as valid zero-crossing signals in generating the symbol clock if judged in the affirmative, and ignores at least one of the N+1 zero-crossing signals in generating the symbol clock if judged in the negative.

3. The clock recovery circuit of claim 2, wherein the clock generation unit includes a circuit operable to adjust a timing of the generated symbol clock based on a phase error with a valid zero-crossing signal, and output the adjusted symbol clock.

4. The clock recovery circuit of claim 2, wherein the clock

generation unit includes a circuit operable to generate a pulse at a center of adjacent zero crossings with reference to a valid zero-crossing signal, adjust a timing of the generated symbol clock based on a phase error with the generated pulse, and output the adjusted symbol clock.

5. The clock recovery circuit of claim 2, wherein $N = 2$, and a minimum time interval of 1 to 2 symbol periods is set as the predetermined interval range.

6. The clock recovery circuit of claim 5, wherein a maximum time interval of 2 to less than 3 symbol periods is set as the predetermined interval range.

7. The clock recovery circuit of claim 2, wherein the N-interval detection unit includes:

a zero-crossing detection subunit operable to detect zero crossings based on the input signal;

a counting subunit operable to measure a time interval between adjacent zero crossings; and

an adding subunit operable to sum N number of adjacent intervals, and output the result as an N-interval control signal.

8. The clock recovery circuit of claim 7, wherein the input signal is an in-phase or quadrature component of a signal obtained by detecting a modulated signal.

9. The clock recovery circuit of claim 6, further comprising:

a 1-interval detection unit operable to detect a 1 zero-crossing interval between adjacent zero-crossings, wherein

the judgment unit judges whether the 1 zero-crossing interval is within a predetermined interval range, and only judges in the affirmative if the 1 zero-crossing interval and the 2 zero-crossing interval are both within respective predetermined interval ranges.

10. The clock recovery circuit of claim 9, wherein the clock generation unit includes a circuit operable to adjust a timing of the generated symbol clock based on a phase error with a valid zero-crossing signal, and output the adjusted symbol clock.

11. The clock recovery circuit of claim 9, wherein the clock generation unit includes a circuit operable to generate a pulse at a center of adjacent zero crossings with reference to a valid zero-crossing signal, adjust a timing of the generated symbol clock based on a phase error with the generated pulse, and output the adjusted symbol clock.

12. A clock recovery circuit for recovering a symbol clock from a signal obtained by detecting a modulated signal, comprising:

an I-component processing unit operable to generate phase error information with reference to an in-phase signal

obtained from the detected signal;

an Q-component processing unit operable to generate phase error information with reference to a quadrature signal obtained from the detected signal; and

a clock generation unit operable to generate and output a symbol clock based on phase error information, wherein

each processing unit includes an *N*-interval detection subunit and an *M*-interval detection subunit (*N*, *M* = positive integers; $N > M$), judges whether an *N* zero-crossing interval and an *M* zero-crossing interval detected by the *N* and *M* interval detection subunits are within respective predetermined interval ranges based on a zero-crossing signal obtained from each of the in-phase signal and the quadrature signal, validates the zero-crossing signal if judged in the affirmative for both the *N* and *M* zero-crossing intervals, and invalidates the zero-crossing signal if judged in the negative for either the *N* or *M* zero-crossing interval, and

if one of the processing units invalidates and the other processing unit validates, the clock generation unit adjusts a phase of the symbol clock based on the phase error information of the validating processing unit, and outputs the phase-adjusted symbol clock.

13. The clock recovery circuit of claim 12, wherein

the modulated signal has a frame structure that includes a preamble, a unique word and data, and

the clock recovery circuit further comprises a

switching circuit operable to output zero-crossing signals validated by the processing units to the clock generation unit as phase error information when the detected signal corresponds to one of the preamble and the unique word, and to output the zero-crossing signals obtained from the in-phase and quadrature signals to the clock generation unit as phase error information when the detected signal corresponds to the data.

14. A receiver for receiving a modulated signal having a frame structure that includes a preamble, a specific pattern and data, comprising:

a signal detection unit operable to detect the received signal, and output an in-phase signal and a quadrature signal;

a phase error correction circuit operable to correct a phase of the in-phase and quadrature signals;

a clock recovery circuit as in claim 12 operable to output a recovered symbol clock to the phase error correction circuit and a data decision unit; and

the data decision unit operable to perform a data decision by synchronizing the phase-corrected signals with the symbol clock.

15. A clock recovery circuit for recovering a symbol clock from an input signal that includes a preamble, comprising:

a zero-crossing detection unit operable to detect a temporal position of zero crossings from the input signal,

and output zero-crossing signals;

an interval detection unit operable to derive a time interval between adjacent zero crossings from the zero-crossing signals, and output interval signals;

a 1-interval judgment unit operable to judge whether each interval signal is within a predetermined interval range;

a 2-interval judgment unit operable to generate a 2-interval signal by summing two adjacent interval signals, and judge whether the 2-interval signal is within a predetermined interval range;

a control unit operable to validate or invalidate each zero-crossing signal based on a judgment result of the judgment units, and output a valid zero-crossing signal; and

a clock generation unit operable to generate a symbol clock based on the valid zero-crossing signal.

16. The clock recovery circuit of claim 15, wherein

the 1-interval judgment unit holds a minimum time interval of 0 to 1 symbol periods and a maximum time interval 1 to 2 symbol periods as the predetermined interval range, and

the 2-interval judgment unit holds a minimum time interval of 1 to 2 symbol periods and a maximum time interval of 2 to less than 3 symbol periods as the predetermined interval range.

17. A receiver for receiving a modulated signal having a frame

structure that includes a preamble, a specific pattern and data, comprising:

a signal detection unit operable to detect the received signal, and output an in-phase signal and a quadrature signal; and

a clock recovery unit operable to recover a symbol clock from the in-phase and quadrature signals, wherein

the clock recovery unit includes:

a frame detection subunit operable to detect the specific pattern from the in-phase and quadrature signals, and output a frame reception signal indicating data reception;

a zero-crossing detection subunit operable to detect a temporal position of zero crossings from the in-phase and quadrature signals, and output in-phase zero-crossing signals and quadrature zero-crossing signals;

an interval detection subunit operable to derive a time interval between adjacent zero crossings from the in-phase and quadrature zero-crossing signals, and output in-phase interval signals and quadrature interval signals;

a 1-interval judgment subunit operable to judge whether each in-phase and quadrature interval signal is within a predetermined interval range;

a 2-interval judgment subunit operable to sum two adjacent in-phase interval signals and two adjacent quadrature interval signals to generate an in-phase 2-interval signal and a quadrature 2-interval signal, and judge whether each in-phase and quadrature 2-interval signal

is within a predetermined interval range;

a control subunit operable to validate or invalidate each in-phase and quadrature zero-crossing signal based on a judgment result of the judgment subunits, and output in-phase and quadrature valid zero-crossing signals;

a switching subunit operable to switch between outputting the in-phase and quadrature zero-crossing signals and the in-phase and quadrature valid zero-crossing signals, based on the frame reception signal; and

a clock generation subunit operable to generate a symbol clock based on the in-phase and quadrature signals output from the switching unit.

18. The receiver of claim 17, wherein

the 1-interval judgment subunit holds a minimum time interval of 0 to 1 symbol periods and a maximum time interval 1 to 2 symbol periods as the predetermined interval range, and

the 2-interval judgment subunit holds a minimum time interval of 1 to 2 symbol periods and a maximum time interval of 2 to less than 3 symbol periods as the predetermined interval range.

19. A receiver for receiving a modulated signal having a frame structure that includes a preamble, a specific pattern and data, comprising:

a signal detection unit operable to detect the received signal, and output an in-phase signal and a quadrature

signal; and

a clock recovery unit operable to recover a symbol clock from the in-phase and quadrature signals, wherein

the clock recovery unit includes:

a frame detection subunit operable to detect the specific pattern from the in-phase and quadrature signals, and output a frame reception signal indicating data reception;

a zero-crossing detection subunit operable to detect a temporal position of zero crossings from the in-phase and quadrature signals, and output in-phase zero-crossing signals and quadrature zero-crossing signals;

an interval detection subunit operable to derive a time interval between adjacent zero crossings from the in-phase and quadrature zero-crossing signals, and output in-phase interval signals and quadrature interval signals;

a center detection subunit operable to detect a temporal position of a center between adjacent in-phase and adjacent quadrature zero-crossing signals, and output in-phase center signals and quadrature center signals;

a 1-interval judgment subunit operable to judge whether each in-phase and quadrature interval signal is within a predetermined interval range;

a 2-interval judgment subunit operable to sum two adjacent in-phase interval signals and two adjacent quadrature interval signals to generate an in-phase 2-interval signal and a quadrature 2-interval signal, and judge whether each in-phase and quadrature 2-interval signal

is within a predetermined interval range;

a control subunit operable to validate or invalidate each in-phase and quadrature center signal based on a judgment result of the judgment subunits, and output in-phase and quadrature valid center signals;

a switching subunit operable to switch between outputting the in-phase and quadrature zero-crossing signals and the in-phase and quadrature valid center signals, based on the frame reception signal; and

a clock generation subunit operable to generate a symbol clock based on the in-phase and quadrature signals output from the switching unit.

20. The receiver of claim 19, wherein

the 1-interval judgment subunit holds a minimum time interval of 0 to 1 symbol periods and a maximum time interval 1 to 2 symbol periods as the predetermined interval range, and

the 2-interval judgment subunit holds a minimum time interval of 1 to 2 symbol periods and a maximum time interval of 2 to less than 3 symbol periods as the predetermined interval range.